ANALOG DEVICES

# Low Cost, 250 mA Output Single-Supply Amplifiers

# AD8531/AD8532/AD8534

**FEATURES**
**Single-Supply Operation: 2.7 Volts to 6 Volts**
**High Output Current: ±250 mA**
**Low Supply Current: 750 μA/Amplifier**
**Wide Bandwidth: 3 MHz**
**Slew Rate: 5 V/μs**
**No Phase Reversal**
**Low Input Currents**
**Unity Gain Stable**

**APPLICATIONS**
**Multimedia Audio**
**LCD Driver**
**ASIC Input or Output Amplifier**
**Headphone Driver**

## GENERAL DESCRIPTION

The AD8531, AD8532 and AD8534 are single, dual and quad rail-to-rail input and output single-supply amplifiers featuring 250 mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth, 5 V/μs slew rate and low distortion. All are guaranteed to operate from a +3 volt single supply as well as a +5 volt supply.

The very low input bias currents enable the AD853x to be used for integrators and diode amplification and other applications requiring low input bias current. Supply current is only 750 μA per amplifier at 5 volts, allowing low current applications to control high current loads.

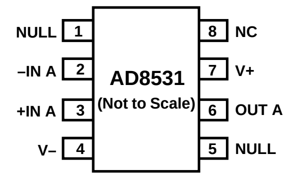
Applications include audio amplification for computers, sound ports, sound cards and set-top boxes. AD853x family is very stable and capable of driving heavy capacitive loads, such as those found in LCDs.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs or other wide output swing devices in single-supply systems.

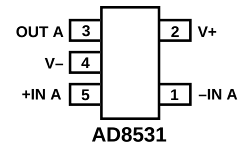
The AD8531, AD8532 and AD8534 are specified over the extended industrial (–40°C to +85°C) temperature range. The AD8531 is available in SO-8 and SOT23-5 packages. The AD8532 is available in 8-pin plastic DIPs, SO-8 and 8-lead TSSOP surface mount packages. The AD8534 is available in 14-pin plastic DIPs, narrow SO-14 are 14-lead TSSOP surface mount packages. All TSSOP and SOT versions are available in tape and reel only.

## PIN CONFIGURATIONS

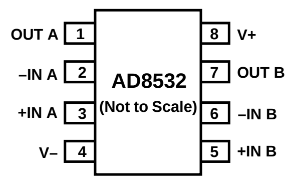
**8-Lead SO (R Suffix)**



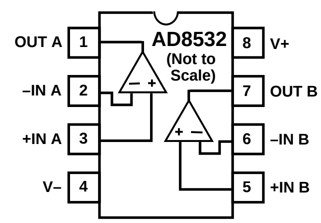

**5-Lead SOT (RT Suffix)**



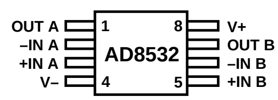

**8-Lead SO (R Suffix)**



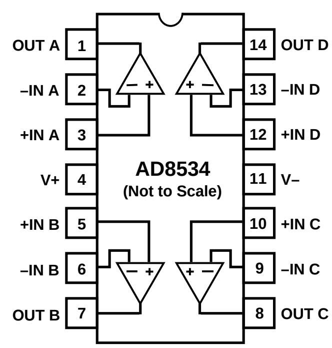

**8-Lead Epoxy DIP (N Suffix)**



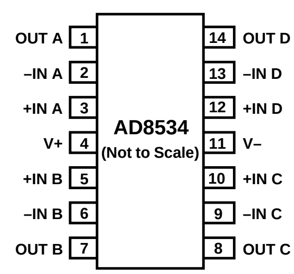

**8-Lead TSSOP (RU Suffix)**



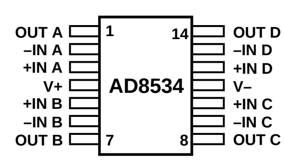

**14-Lead Epoxy DIP (N Suffix)**




**14-Lead Narrow-Body SO (R Suffix)**




**14-Lead TSSOP (RU Suffix)**




REV. 0



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

# AD8531/AD8532/AD8534–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = +3.0 V, $V_{CM}$ = 1.5 V, $T_A$ = +25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | | 25 | mV |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 30 | mV |
| Input Bias Current | $I_B$ | | | 5 | 50 | pA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 60 | pA |
| Input Offset Current | $I_{OS}$ | | | 1 | 25 | pA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 30 | pA |
| Input Voltage Range | | | 0 | | 3 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 3 V | 38 | 45 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 2.5 V | | 25 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 20 | | µV/°C |
| Bias Current Drift | $\Delta I_B/\Delta T$ | | | 50 | | fA/°C |
| Offset Current Drift | $\Delta I_{OS}/\Delta T$ | | | 20 | | fA/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 10 mA | 2.85 | 2.92 | | V |
| | | –40°C ≤ $T_A$ ≤ +85°C | 2.8 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 10 mA | | 60 | 100 | mV |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 125 | mV |
| Output Current | $I_{OUT}$ | | | ±250 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 60 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 3 V to 6 V | 45 | 55 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | | 1 | mA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 1.25 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 3.5 | | V/µs |
| Settling Time | $t_S$ | To 0.01% | | 1.4 | | µs |
| Gain Bandwidth Product | GBP | | | 2.2 | | MHz |
| Phase Margin | φo | | | 70 | | Degrees |
| Channel Separation | CS | f = 1 kHz, $R_L$ = 2 kΩ | | 65 | | dB |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 45 | | $nV/\sqrt{Hz}$ |
| Voltage Noise Density | $e_n$ | f = 10 kHz | | 30 | | $nV/\sqrt{Hz}$ |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.05 | | $pA/\sqrt{Hz}$ |

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = +5.0 V, $V_{CM}$ = 2.5 V, $T_A$ = +25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | $V_{OS}$ | | | | 25 | mV |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 30 | mV |
| Input Bias Current | $I_B$ | | | 5 | 50 | pA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 60 | pA |
| Input Offset Current | $I_{OS}$ | | | 1 | 25 | pA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 30 | pA |
| Input Voltage Range | | | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 5 V | 38 | 47 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 4.5 V | 15 | 80 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | –40°C ≤ $T_A$ ≤ +85°C | | 20 | | µV/°C |
| Bias Current Drift | $\Delta I_B/\Delta T$ | | | 50 | | fA/°C |
| Offset Current Drift | $\Delta I_{OS}/\Delta T$ | | | 20 | | fA/°C |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 10 mA | 4.9 | 4.94 | | V |
| | | –40°C ≤ $T_A$ ≤ +85°C | 4.85 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 10 mA | | 50 | 100 | mV |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 125 | mV |
| Output Current | $I_{OUT}$ | | | ±250 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 40 | | Ω |
| **POWER SUPPLY** | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 3 V to 6 V | 45 | 55 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | 1.4 | 1.25 | mA |
| | | –40°C ≤ $T_A$ ≤ +85°C | | | 1.75 | mA |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 5 | | V/µs |
| Full-Power Bandwidth | $BW_p$ | 1% Distortion | | 350 | | kHz |
| Settling Time | $t_S$ | To 0.01% | | 1.6 | | µs |
| Gain Bandwidth Product | GBP | | | 3 | | MHz |
| Phase Margin | $\phi o$ | | | 70 | | Degrees |
| Channel Separation | CS | f = 1 kHz, $R_L$ = 2 kΩ | | 65 | | dB |
| **NOISE PERFORMANCE** | | | | | | |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 45 | | $nV/\sqrt{Hz}$ |
| Voltage Noise Density | $e_n$ | f = 10 kHz | | 30 | | $nV/\sqrt{Hz}$ |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.05 | | $pA/\sqrt{Hz}$ |

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_S$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . +7 V
Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . GND to $V_S$
Differential Input Voltage[1] . . . . . . . . . . . . . . . . . . . . . . . ±6 V
Storage Temperature Range
  N, R, RT, RU Package . . . . . . . . . . . . . . . –65°C to +150°C
Operating Temperature Range
  AD8531/AD8532/AD8534 . . . . . . . . . . . . . –40°C to +85°C
Junction Temperature Range
  N, R, RT, RU Package . . . . . . . . . . . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . . +300°C

### PACKAGE INFORMATION

| Package Type | $\theta_{JA}$[2] | $\theta_{JC}$ | Units |
|---|---|---|---|
| 5-Lead SOT-23 (RT) | 230 | | °C/W |
| 8-Pin SOIC (R) | 158 | 43 | °C/W |
| 8-Pin TSSOP (RU) | 240 | 43 | °C/W |
| 14-Pin Plastic DIP (N) | 83 | 39 | °C/W |
| 14-Pin SOIC (R) | 120 | 36 | °C/W |
| 14-Pin TSSOP (RU) | 240 | 43 | °C/W |

NOTES
[1]For supplies less than +6 volts, the differential input voltage is equal to $\pm V_S$.
[2]$\theta_{JA}$ is specified for the worst case conditions, i.e., $\theta_{JA}$ is specified for device in socket for P-DIP packages; $\theta_{JA}$ is specified for device soldered onto a circuit board for surface mount packages.

### ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8531AR | –40°C to +85°C | 8-Pin SOIC | SO-8 |
| AD8531ART[1] | –40°C to +85°C | 5-Lead SOT-23 | RT-5 |
| AD8532AR | –40°C to +85°C | 8-Pin SOIC | SO-8 |
| AD8532AN | –40°C to +85°C | 8-Pin Plastic DIP | N-8 |
| AD8532ARU[2] | –40°C to +85°C | 8-Pin TSSOP | RU-8 |
| AD8534AR | –40°C to +85°C | 14-Pin SOIC | SO-14 |
| AD8534AN | –40°C to +85°C | 14-Pin Plastic DIP | N-14 |
| AD8534ARU[2] | –40°C to +85°C | 14-Pin TSSOP | RU-14 |

NOTES
[1]Available in 2,500 piece reels only.
[2]Available in 2,500 piece reels only.

### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8531/AD8532/AD8534 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



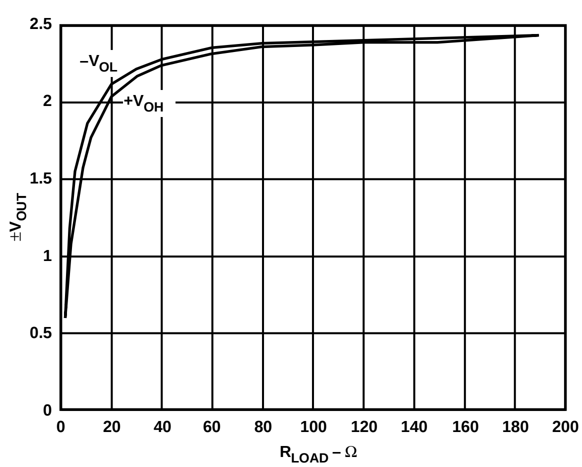




*Figure 1. Output Voltage vs. Load. $V_S = \pm 2.5$ V, $R_L$ Is Connected to GND (0 V)*

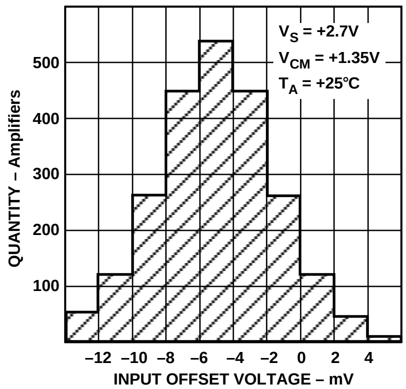



*Figure 2. Input Offset Voltage Distribution*

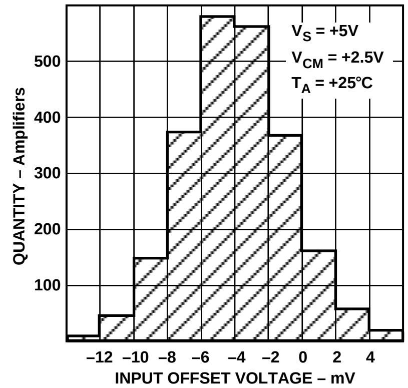



*Figure 3. Input Offset Voltage Distribution*

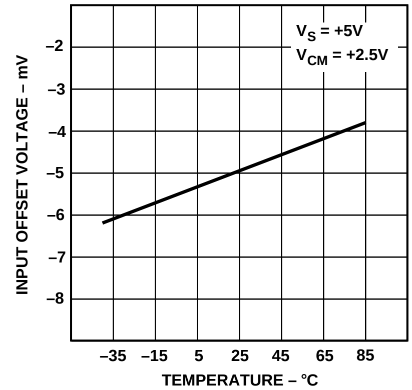



*Figure 4. Input Offset Voltage vs. Temperature*

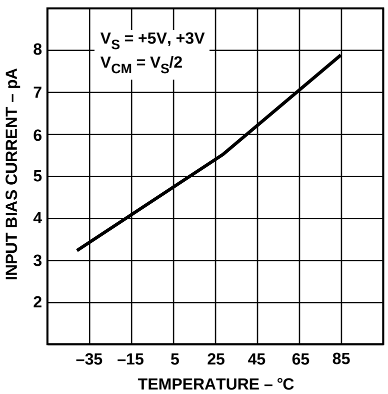



*Figure 5. Input Bias Current vs. Temperature*

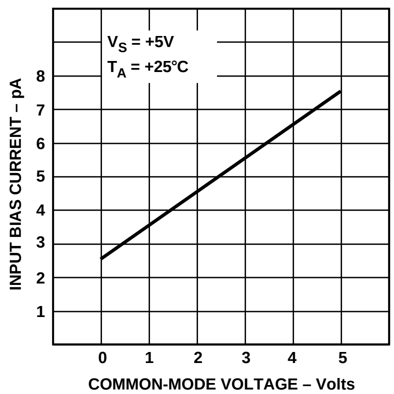



*Figure 6. Input Bias Current vs. Common-Mode Voltage*

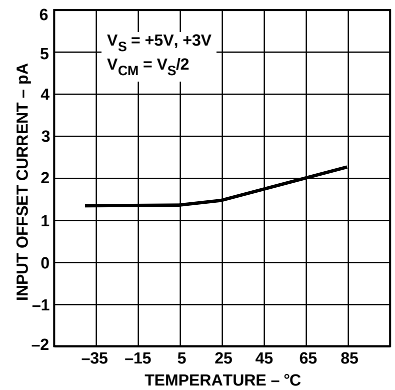



*Figure 7. Input Offset Current vs. Temperature*

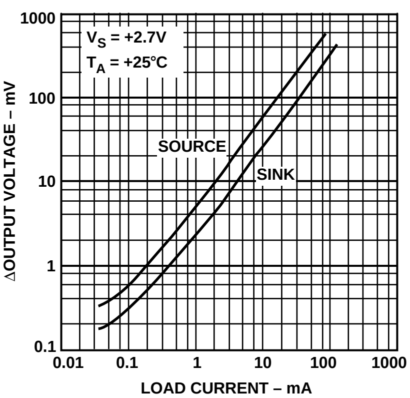



*Figure 8. Output Voltage to Supply Rail vs. Load Current*

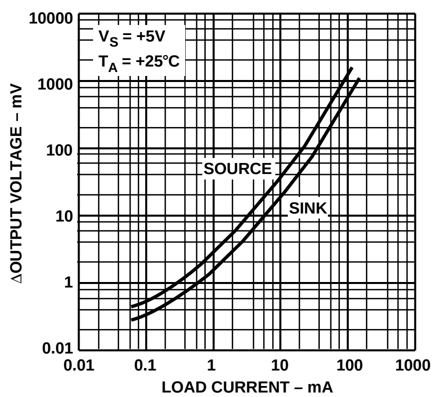



*Figure 9. Output Voltage to Supply Rail vs. Load Current*

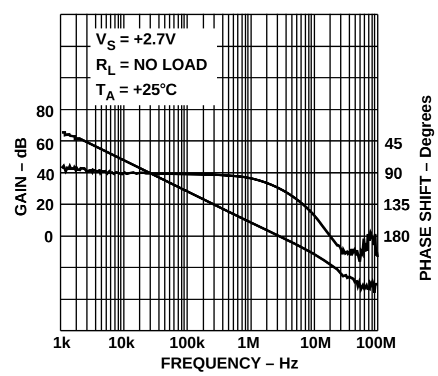



*Figure 10. Open-Loop Gain & Phase vs. Frequency*

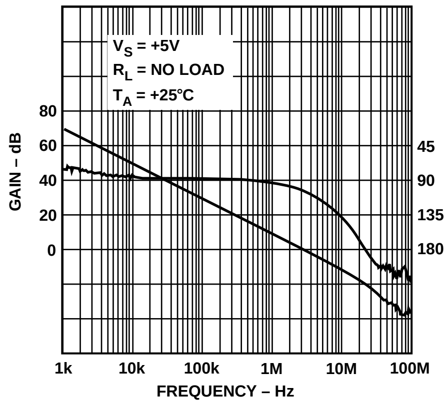



Figure 11. Open-Loop Gain & Phase vs. Frequency

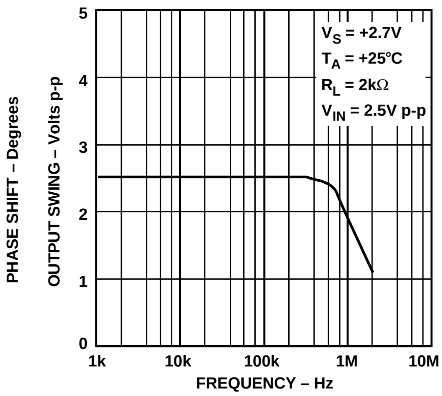



Figure 12. Closed-Loop Output Voltage Swing vs. Frequency

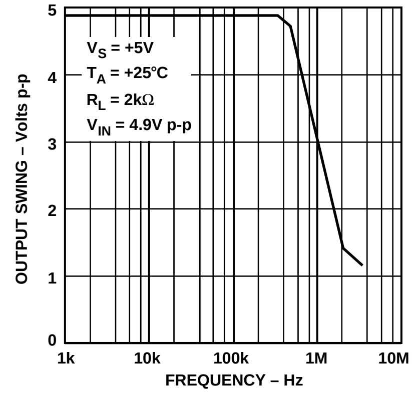



Figure 13. Closed-Loop Output Voltage Swing vs. Frequency

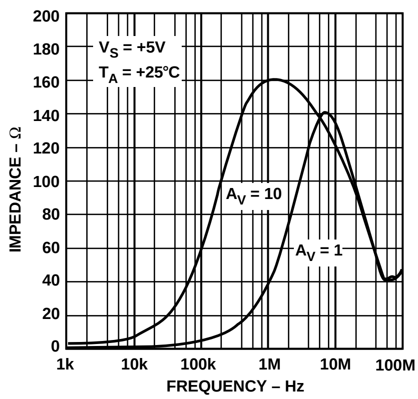



Figure 14. Closed-Loop Output Impedance vs. Frequency

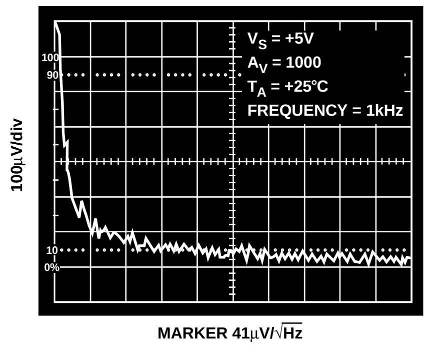



Figure 15. Voltage Noise Density vs. Frequency

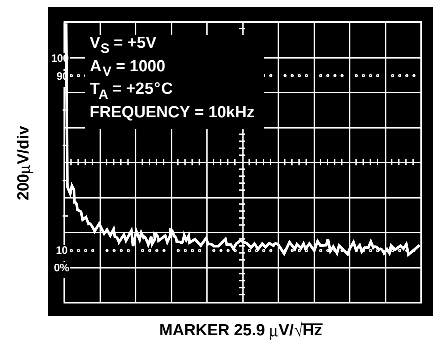



Figure 16. Voltage Noise Density vs. Frequency

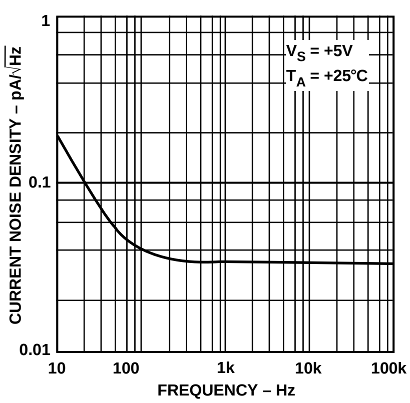



Figure 17. Current Noise Density vs. Frequency

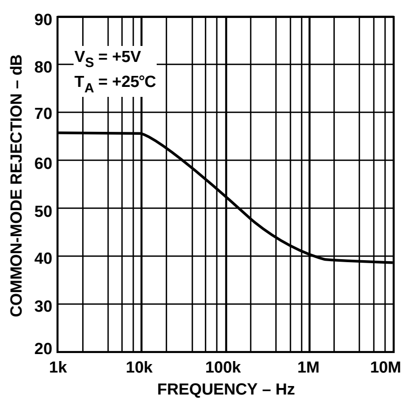



Figure 18. Common-Mode Rejection vs. Frequency

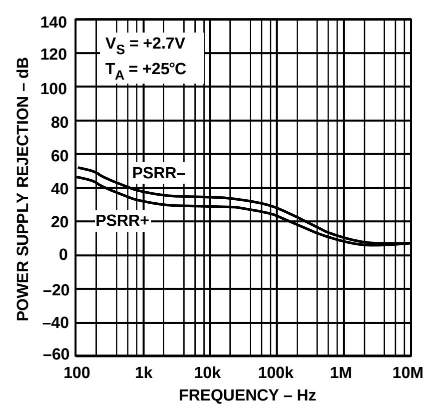



Figure 19. Power Supply Rejection vs. Frequency

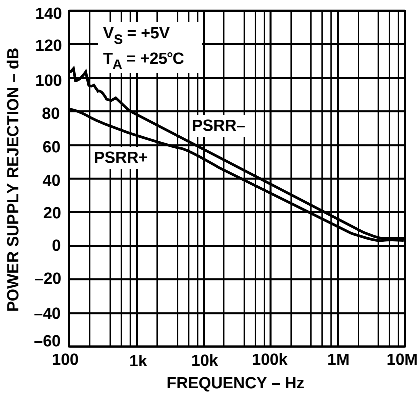



*Figure 20. Power Supply Rejection vs. Frequency*

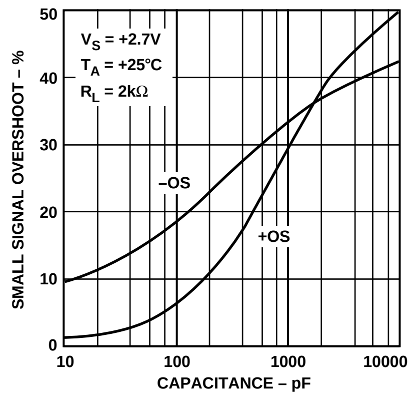



*Figure 21. Small Signal Overshoot vs. Load Capacitance*

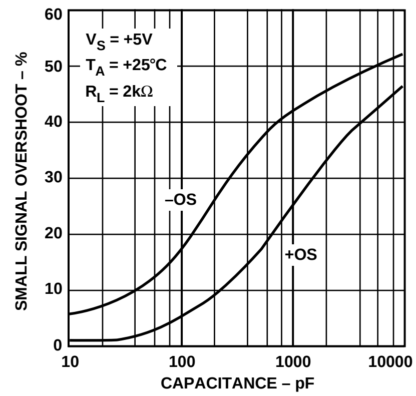



*Figure 22. Small Signal Overshoot vs. Load Capacitance*

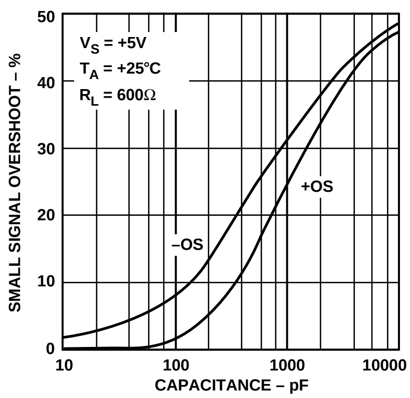



*Figure 23. Small Signal Overshoot vs. Load Capacitance*

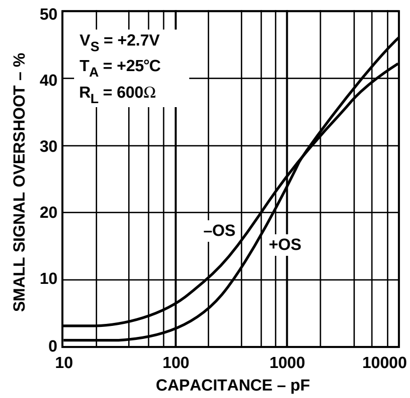



*Figure 24. Small Signal Overshoot vs. Load Capacitance*

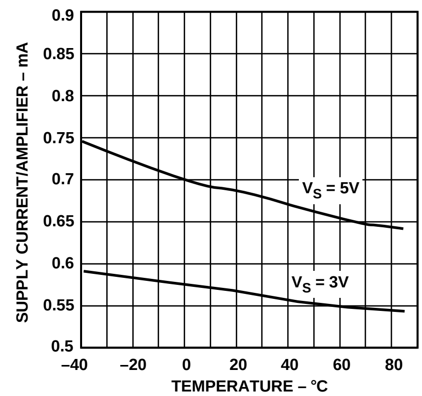



*Figure 25. Supply Current per Amplifier vs. Temperature*

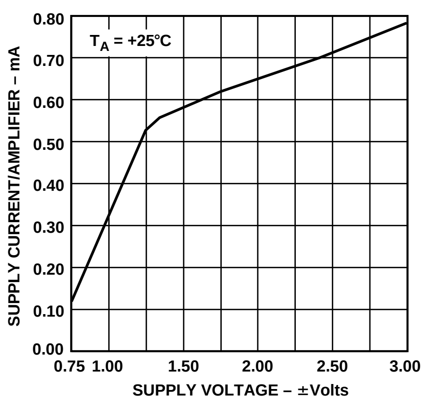



*Figure 26. Supply Current per Amplifier vs. Supply Voltage*

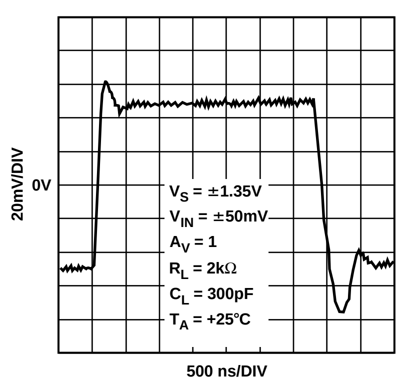



*Figure 27. Small Signal Transient Response*

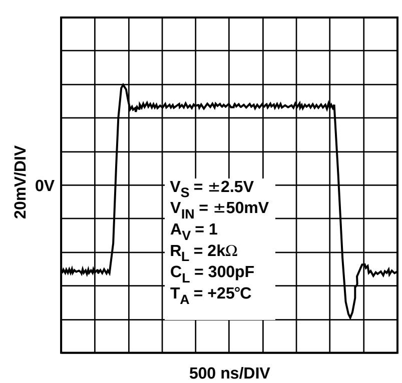



*Figure 28. Small Signal Transient Response*

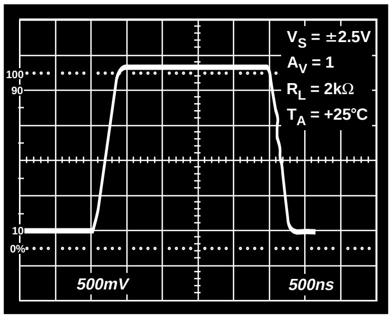



Figure 29. Large Signal Transient Response

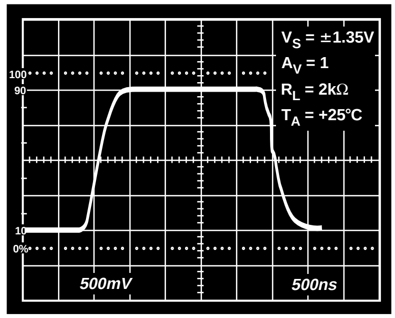



Figure 30. Large Signal Transient Response

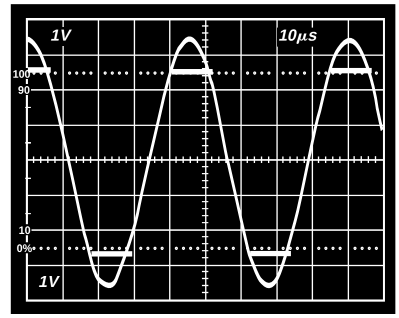



Figure 31. No Phase Reversal

## APPLICATIONS

### THEORY OF OPERATION

The AD8531/AD8532/AD8534 is an all-CMOS, high output current drive, rail-to-rail input/output operational amplifier. This is the latest entry in Analog Devices' expanding family of single-supply devices for the multimedia and telecom marketplaces. Its high output current drive and stability with heavy capacitive loads makes the AD8531/AD8532/AD8534 an excellent choice as a drive amplifier for LCD panels.

Figure 32 illustrates a simplified equivalent circuit for the AD8531/AD8532/AD8534. Like many rail-to-rail input amplifier configurations, it is comprised of a two differential pairs, one n-channel (M1–M2) and one p-channel (M3–M4). These differential pairs are biased by 50 µA current sources, each with a compliance limit of approximately 0.5 V from either supply voltage rail. The differential input voltage is then converted into a pair of differential output currents. These differential output currents are then combined together in a compound folded-cascode second gain stage (M5–M9). The outputs of the second gain stage at M8 and M9 provide the gate voltage drive to the rail-to-rail, output stage. Additional signal current recombination for the output stage is achieved through the use of transistors M11–M14.

In order to achieve rail-to-rail output swings, the AD8531/AD8532/AD8534 design employs a complementary common-source output stage (M15–M16). However, the output voltage swing is directly dependent on the load current, as the difference between the output voltage and the supply is determined by the AD8531/AD8532/AD8534's output transistors on-channel resistance (see Figures 8 and 9). The output stage also exhibits voltage gain by virtue of the use of common-source amplifiers; and as a result the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a strong dependence to the total load resistance at the output of the AD8531/AD8532/AD8534.

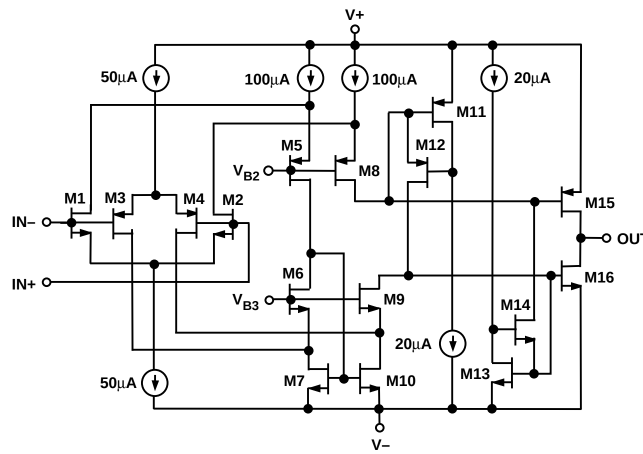



Figure 32. AD8531/AD8532/AD8534 Simplified Equivalent Circuit

### Short-Circuit Protection

As a result of the design of the output stage for maximum load current capability, the AD8531/AD8532/AD8534 does not have any internal short-circuit protection circuitry. Direct connection of the AD8531/AD8532/AD8534's output to the positive supply in single-supply applications will destroy the device. In those applications where some protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output, as shown in Figure 33, can be used. The resistor, connected within the feedback loop of the amplifier, will have very little effect on the performance of the amplifier other than limiting the maximum available output voltage swing. For single +5 V supply applications, resistors less than 20 Ω are not recommended.

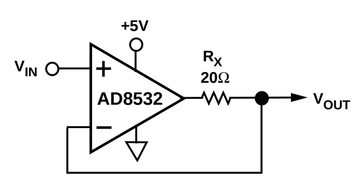



Figure 33. Output Short-Circuit Protection

**Power Dissipation**

Although the AD8531/AD8532/AD8534 is capable of providing load currents to 250 mA, the usable output load current drive capability will be limited to the maximum power dissipation allowed by the device package used. In any application, the absolute maximum junction temperature for the AD8531/AD8532/AD8534 is 150°C, and should never be exceeded for the device could suffer premature failure. Accurately measuring power dissipation of an integrated circuit is not always a straightforward exercise, so Figure 34 has been provided as a design aid for either setting a safe output current drive level or in selecting a heat sink for the three package options available on the AD8531/AD8532/AD8534.

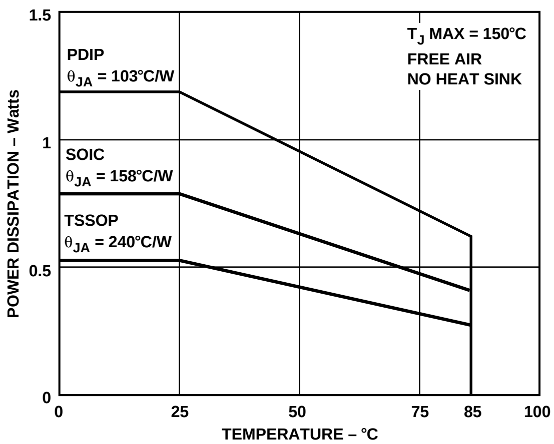



*Figure 34. Maximum Power Dissipation vs. Ambient Temperature*

These thermal resistance curves were determined using the AD8531/AD8532/AD8534 thermal resistance data for each package and a maximum junction temperature of 150°C. The following formula can be used to calculate the internal junction temperature of the AD8531/AD8532/AD8534 for any application:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where $T_J$ = junction temperature;
$P_{DISS}$ = power dissipation;
$\theta_{JA}$ = package thermal resistance, junction-to-case; and
$T_A$ = Ambient temperature of the circuit.

To calculate the power dissipated by the AD8531/AD8532/AD8534, the following equation can be used:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where $I_{LOAD}$ = is output load current;
$V_S$ = is supply voltage; and
$V_{OUT}$ = is output voltage.

The quantity within the parentheses is the maximum voltage developed across either output transistor. As an additional design aid in calculating available load current from the AD8531/AD8532/AD8534, Figure 1 illustrates the AD8531/AD8532/AD8534 output voltage as a function of load resistance.

**Power Calculations for Varying or Unknown Loads**

Often, calculating power dissipated by an integrated circuit to determine if the device is being operated in a safe range is not as simple as it might seem. In many cases power cannot be measured directly. This may be the result of irregular output waveforms or varying loads. So indirect methods of measuring power are required.

Here are two methods to calculate power dissipated by an integrated circuit. The first can be done by measuring the package temperature and the board temperature. The other method is to directly measure the circuit's supply current.

**Calculating Power by Measuring Ambient and Case Temperature**

Given the two equations for calculating junction temperature:

$$T_J = T_A + P\,\theta_{JA}$$

where $T_J$ is junction temperature, and $T_A$ is ambient temperature. $\theta_{JA}$ is the junction to ambient thermal resistance.

$$T_J = T_C + P\,\theta_{JC}$$

where $T_C$ is case temperature and $\theta_{JA}$ and $\theta_{JC}$ are given in the data sheet.

The two equations can be solved for *P* (power):

$$T_A + P\,\theta_{JA} = T_C + P\,\theta_{JC}$$

$$P = (T_A - T_C)/(\theta_{JC} - \theta_{JA})$$

Once power has been determined it is necessary to go back and calculate the junction temperature to assure that it has not been exceeded.

The temperature measurements should be directly on the package and on a spot on the board that is near the package but definitely not touching it. Measuring the package could be difficult. A very small bimetallic junction glued to the package could be used or it could be done using an infrared sensing device if the spot size is small enough.

**Calculating Power by Measuring Supply Current**

Power can be calculated directly knowing the supply voltage and current. However, supply current may have a dc component with a pulse into a capacitive load. This could make rms current very difficult to calculate.

This can be overcome by lifting the supply pin and inserting an rms current meter into the circuit. For this to work you must be sure all of the current is being delivered by the supply pin that you are measuring. This is usually a good method in a single supply system. However, if the system uses dual supplies, both supplies may need to be monitored.

**Input Overvoltage Protection**

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, the device's input overvoltage characteristic must be considered. When an overvoltage occurs, the amplifier could be damaged depending on the magnitude of the applied voltage and the magnitude of the fault current. Although not shown here, when the input voltage exceeds either supply by more than 0.6 V, pn-junctions internal to the AD8531/AD8532/AD8534 energize allowing current to flow from the input to the supplies. As illustrated in the simplified equivalent input circuit (Figure 32), the AD8531/AD8532/AD8534 does not have any internal current limiting resistors, so fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. For the AD8531/AD8532/AD8534, once the input voltage exceeds the supply by more than 0.6 V the input current quickly exceeds 5 mA. If this

condition continues to exist, an external series resistor should be added. The size of the resistor is calculated by dividing the maximum overvoltage by 5 mA. For example, if the input voltage could reach 10 V, the external resistor should be (10 V/5 mA) = 2 kΩ. This resistance should be placed in series with either or both inputs if they are exposed to an overvoltage condition. For more information on general overvoltage characteristics of amplifiers refer to the *1993 Seminar Applications Guide*, available from the Analog Devices Literature Center.

**Output Phase Reversal**

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. The AD8531/AD8532/AD8534 is free from reasonable input voltage range restrictions provided that the input voltages no greater than the supply voltage rails are applied. Although the device's output will not change phase, large currents can flow through internal junctions to the supply rails, as was pointed out in the previous section. Without limit, these fault currents can easily destroy the amplifier. Therefore, the technique recommended in the input overvoltage protection section should be applied in those applications where the possibility of input voltages exceeding the supply voltages exists.

**Capacitive Load Drive**

The AD8531/AD8532/AD8534 exhibits excellent capacitive load driving capabilities. It can drive up to 10 nF directly as shown in Figures 21 through 24. However, even though the device is stable, a capacitive load does not come without a penalty in bandwidth. As shown in Figure 35, the bandwidth is reduced to under 1 MHz for loads greater than 10 nF. A "snubber" network on the output won't increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load. A snubber consists of a series R-C network ($R_S$, $C_S$), as shown in Figure 36, connected from the output of the device to ground. This network operates in parallel with the load capacitor, $C_L$, to provide phase lag compensation. The actual value of the resistor and capacitor is best determined empirically.

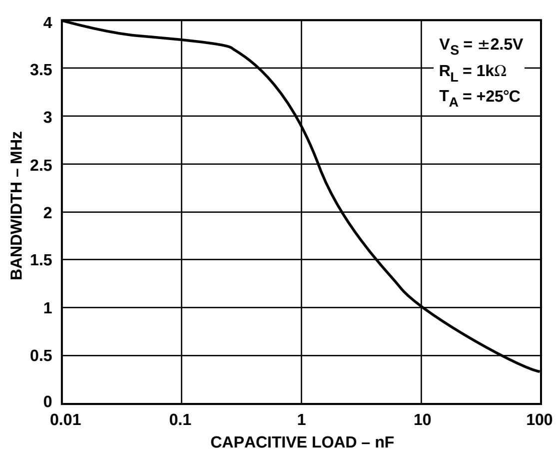



*Figure 35. Unity-Gain Bandwidth vs. Capacitive Load*

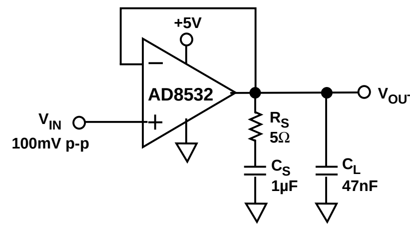



*Figure 36. Snubber Network Compensates for Capacitive Loads*

The first step is to determine the value of the resistor, $R_S$. A good starting value is 100 Ω. This value is reduced until the small-signal transient response is optimized. Next, $C_S$ is determined—10 µF is a good starting point. This value is reduced to the smallest value for acceptable performance (typically, 1 µF). For the case of a 47 nF load capacitor on the AD8531/AD8532/AD8534, the optimal snubber network is a 5 Ω in series with 1 µF. The benefit is immediately apparent as seen in the scope photo in Figure 37. The top trace was taken with a 47 nF load and the bottom trace with the 5 Ω—1 µF snubber network in place. The amount of overshoot and ringing is dramatically reduced. Table I below illustrates a few sample snubber networks for large load capacitors:

**Table I. Snubber Networks for Large Capacitive Loads**

| Load Capacitance ($C_L$) | Snubber Network ($R_S$, $C_S$) |
|---|---|
| 0.47 nF | 300 Ω, 0.1 µF |
| 4.7 nF | 30 Ω, 1 µF |
| 47 nF | 5 Ω, 1 µF |

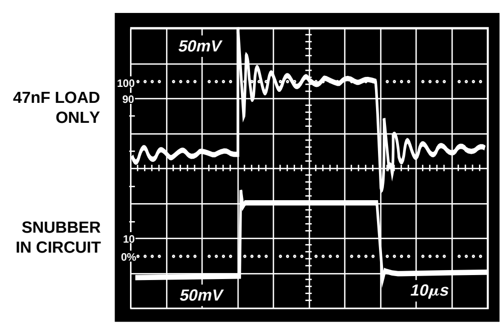



*Figure 37. Overshoot and Ringing Is Reduced by Adding a Snubber Network in Parallel with the 47 nF Load*

**A High Output Current, Buffered Reference/Regulator**

Many applications require stable voltage outputs relatively close in potential to an unregulated input source. This "low dropout" type of reference/regulator is readily implemented with a rail-to-rail output op amp, and is particularly useful when using a higher current device such as the AD8531/AD8532/AD8534. A typical example is the 3.3 V or 4.5 V reference voltage developed from a 5 V system source. Generating these voltages requires a three terminal reference, such as the REF196 (3.3 V) or the REF194 (4.5 V), both which feature low power, with sourcing outputs of 30 mA or less. Figure 38 shows how such a reference can be outfitted with an AD8531/AD8532/AD8534 buffer for higher currents and/or voltage levels, plus sink and source load capability.

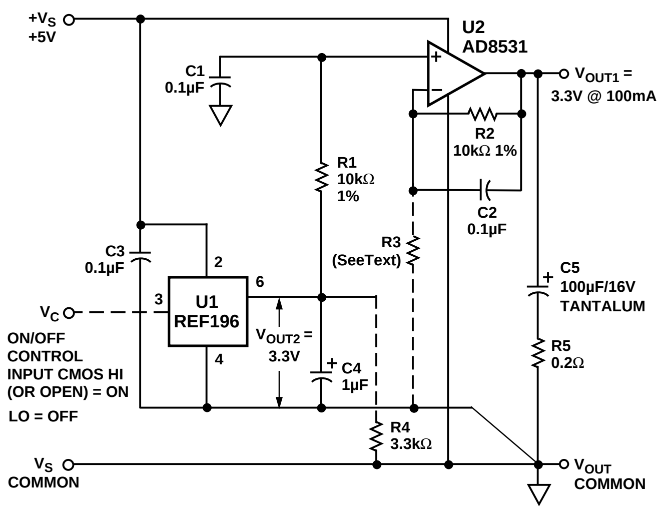



*Figure 38. A High Output Current Reference/Regulator*

The low dropout performance of this circuit is provided by stage U2, an AD8531 connected as a follower/buffer for the basic reference voltage produced by U1. The low voltage saturation characteristic of the AD8531/AD8532/AD8534 allows up to 100 mA of load current in the illustrated use, as a 5 V to 3.3 V converter with good dc accuracy. In fact, the dc output voltage change for a 100 mA load current delta measured less than 1 mV. This corresponds to an equivalent output impedance of < 0.01 Ω. In this application, the stable 3.3 V from U1 is applied to U2 through a noise filter, R1–C1. U2 replicates the U1 voltage within a few millivolts, but at a higher current output at $V_{OUT1}$, with the ability to both sink and source output current(s) —unlike most IC references. R2 and C2 in the feedback path of U2 provide additional noise filtering.

Transient performance of the reference/regulator for a 100 mA step change in load current is also quite good and is determined largely by the R5–C5 output network. With values as shown, the transient is about 20 mV peak and settles to within 2 mV in less than 10 µs for either polarity. Although there exists room for optimizing the transient response, any changes to the R5–C5 network should be verified by experiment to preclude the possibility of excessive ringing with some capacitor types.

To scale $V_{OUT2}$ to another (higher) output level, the optional resistor R3 (shown dotted) is added causing the new $V_{OUT1}$ to become:

$$V_{OUT1} = V_{OUT2} \times \left(1 + \frac{R2}{R3}\right)$$

The circuit can be used either as shown as a 5 V to 3.3 V reference/regulator, or it can also be used with ON/OFF control. By driving Pin 3 of U1 with a logic control signal as noted, the output is switched ON/OFF. Note that when ON/OFF control is used, resistor R4 must be used with U1, to speed ON-OFF switching.

**A Single-Supply, Balanced Line Driver**

The circuit in Figure 39 is a unique line driver circuit topology used in professional audio applications and has been modified for the automotive and multimedia audio applications. On a single +5 V supply, the line driver exhibits less than 0.7% distortion into a 600 Ω load from 20 Hz to 15 kHz (not shown) with an input signal level of 4 V p-p. In fact, the output drive capability of the AD8531/AD8532/AD8534 maintains this level for loads as small as 32 Ω. For input signals less than 1 V p-p, the THD is less than 0.1%, regardless of load. The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based system, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily configured for noninverting, inverting, or differential operation.

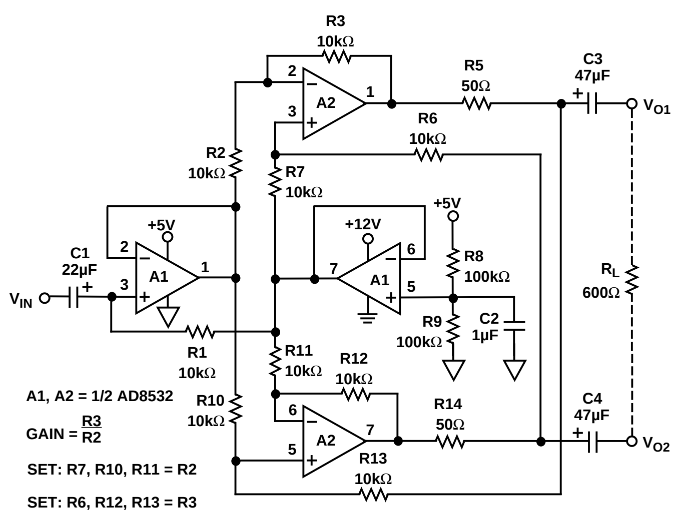



*Figure 39. A Single-Supply, Balanced Line Driver for Multimedia and Automotive Applications*

**A Single-Supply Headphone Amplifier**

Because of its speed and large output drive, the AD8531/AD8532/AD8534 makes for an excellent headphone driver, as illustrated in Figure 40. Its low supply operation and rail-to-rail inputs and outputs give a maximum signal swing on a single +5 V supply. To insure maximum signal swing available to drive the headphone, the amplifier inputs are biased to V+/2, which is in this case 2.5 V. The 100 kΩ resistor to the positive supply is equally split into two 50 kΩ resistors with their common point bypassed by 10 µF to prevent power supply noise from contaminating the audio signal.

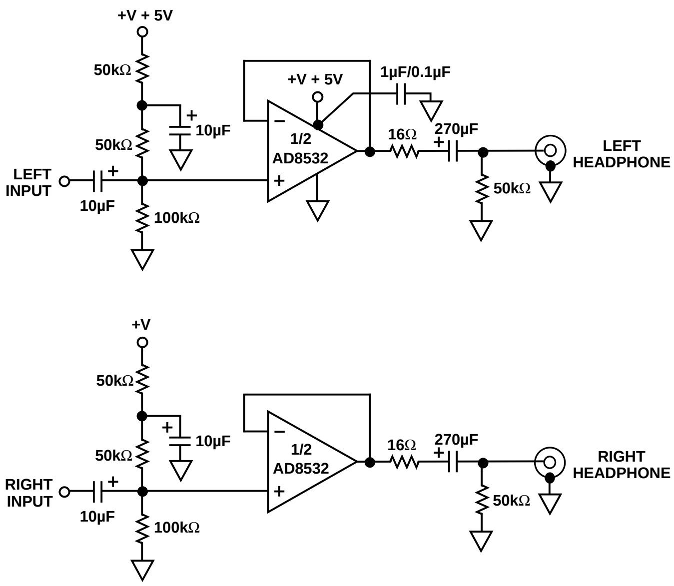



*Figure 40. A Single-Supply, Stereo Headphone Driver*

The audio signal is then ac-coupled to each input through a 10 µF capacitor. A large value is needed to ensure that the 20 Hz audio information is not blocked. If the input already has the proper dc bias, then the ac coupling and biasing resistors are not required. A 270 µF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of the headphones, which can range from 32 Ω to 600 Ω. An additional 16 Ω resistor is used in series with the output capacitor to protect the op amp's output stage by limiting capacitor discharge current. When driving a 48 Ω load, the circuit exhibits less than 0.3% THD+N at output drive levels of 4 V p-p.

**A Single-Supply, Two-Way Loudspeaker Crossover Network**

Active filters are useful in loudspeaker crossover networks for reasons of small size, relative freedom from parasitic effects, and the ease of controlling low/high channel drive, plus the controlled driver damping provided by a dedicated amplifier. Both Sallen-Key (SK) and multiple-feedback (MFB) filter architectures are useful in implementing active crossover networks. The circuit shown in Figure 41 is a single-supply, two-way active crossover which combines the advantages of both filter topologies. This active crossover exhibits less than 0.4% THD+N at output levels of 1.4 V rms using general purpose unity-gain HP/LP stages.

In this two-way example, the LO signal is a dc-500 Hz LP woofer output, and the HI signal is the HP (>500 Hz) tweeter output. U1B forms an LP section at 500 Hz, while U1A provides a HP section, covering frequencies ≥500 Hz.

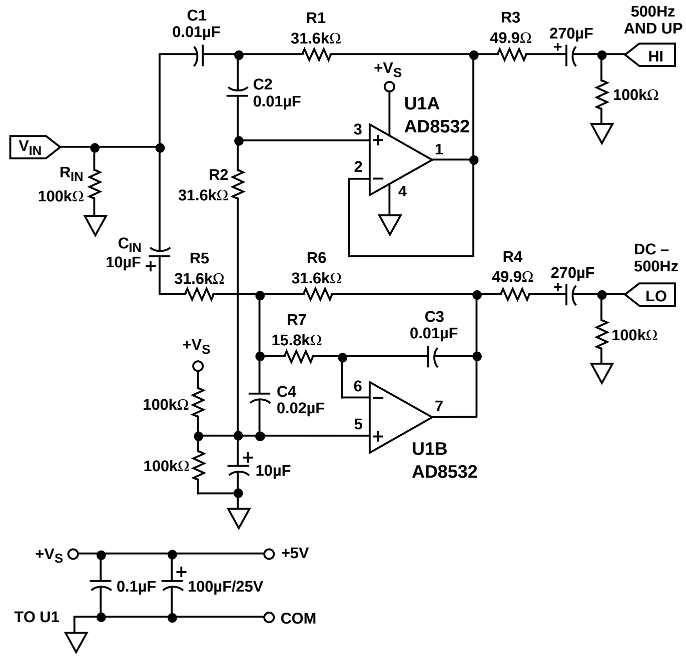



*Figure 41. A Single-Supply, Two-Way Active Crossover*

The crossover example frequency of 500 Hz can be shifted lower or higher by frequency scaling of either resistors or capacitors. In configuring the circuit for other frequencies, complementary LP/HP action must be maintained between sections, and component values within the sections must be in the same ratio. Table II provides a design aid to adaptation, with suggested standard component values for other frequencies.

**Table II. RC Component Selection for Various Crossover Frequencies**

| Crossover Frequency (Hz) | R1/C1 (U1A)[1] R5/C3 (U1B)[2] |
|---|---|
| 100 | 160 kΩ/0.01 µF |
| 200 | 80.6 kΩ/0.01 µF |
| 319 | 49.9 kΩ/0.01 µF |
| 500 | 31.6 kΩ/0.01 µF |
| 1 k | 16 kΩ/0.01 µF |
| 2 k | 8.06 kΩ/0.01 µF |
| 5 k | 3.16 kΩ/0.01 µF |
| 10 k | 1.6 kΩ/0.01 µF |

NOTES

Applicable for filter α = 2.

[1]For Sallen-Key stage U1A: R1 = R2, and C1 = C2, etc.

[2]For Multiple Feedback stage U1B: R6 = R5, R7 = R5/2, and C4 = 2C3.

For additional information on the active filters and active crossover networks, please consult the data sheet for the OP279, a dual rail-to-rail high-output current operational amplifier.

**Direct Access Arrangement for Telephone Line Interface**

Figure 42 illustrates a +5 V only transmit/receive telephone line interface for 600 Ω transmission systems. It allow full duplex transmission of signals on a transformer coupled 600 Ω line in a differential manner. Amplifier A1 provides gain which can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured so as to apply the largest possible signal on a single supply to the transformer. Because of the AD8531/AD8532/AD8534's high output current drive and low dropout voltage, the largest signal available on a single +5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal, and (2) it extracts the receive signal from the transmission line for amplification by A4. A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the AD8531/AD8532/AD8534's 8-pin SOIC or TSSOP footprint and this circuit offers a compact, cost-sensitive solution.

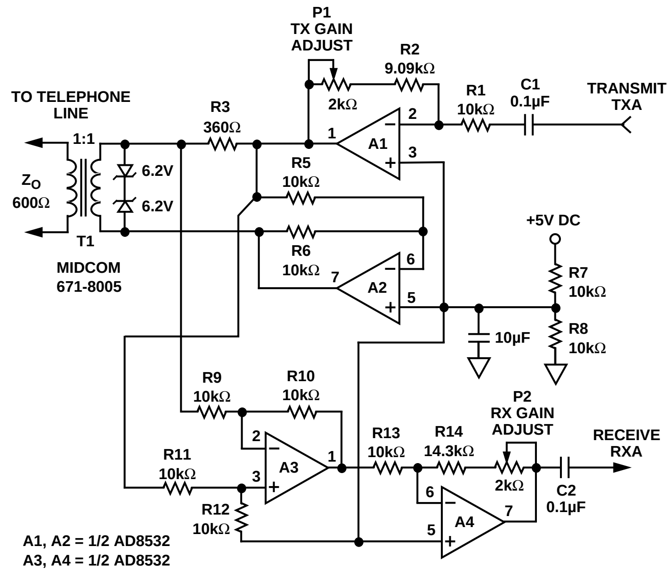


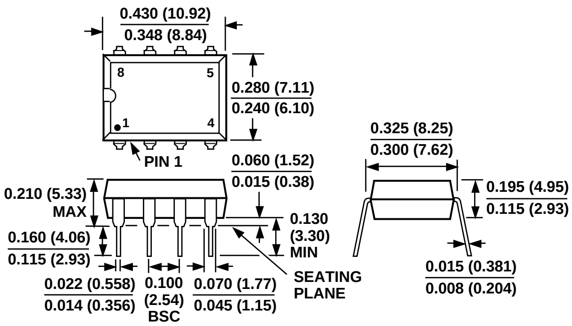

*Figure 42. A Single-Supply Direct Access Arrangement for Modems*

```
* AD8531/AD8532/AD8534 SPICE Macro-model            3/96, Rev. A
* 5-Volt Version                        ARG / ADSC
*
* Copyright 1996 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of this model
* indicates your acceptance of the terms and provisions in the License
* Statement.
*
* Node assignments
*                                       noninverting input
*                                       |    inverting input
*                                       |    |    positive supply
*                                       |    |    |    negative supply
*                                       |    |    |    |    output
*                                       |    |    |    |    |
.SUBCKT AD8531/AD8532/AD8534_5          1    2    99   50   40
*
* INPUT STAGE
*
M1      3     2     6         50    NIX   L=6U W=25U
M2      4     7     6         50    NIX   L=6U W=25U
M3      8     2     5         5     PIX   L=6U W=25U
M4      9     7     5         5     PIX   L=6U W=25U
EOS     7     1     POLY(1)   25    98    5E-3  0.451
IIN1    1     98    5P
IIN2    2     98    5P
IOS     2     1     0.5P
I1      99    5     50U
I2      6     50    50U
R1      99    3     4.833K
R2      99    4     4.833K
R3      8     50    4.833K
R4      9     50    4.833K
D3      5     99    DX
D4      50    6     DX
*
* GAIN  STAGE
*
EREF    98    0     POLY(2)   99    0     50    0     0     0.5
+0.5
G1      98    21    POLY(2)   4     3     9     8     0
+145U   +145U
RG      21    98    18.078E6
CC      21    40    14P
D1      21    22    DX
D2      23    21    DX
V1      99    22    1.37
V2      23    50    1.37
*
* COMMON MODE GAIN STAGE
*
ECM     24    98    POLY(2)   1     98    2     98    0     0.5
+0.5
R5      24    25    1E6
R6      25    98    10K
C1      24    25    0.75P
*
* OUTPUT STAGE
*
ISY     99    50    450.4U
GSY     99    50    POLY(1)   99    50    -3.334E-4   6.667E-5
EP      99    39    POLY(1)   98    21    0.78925     1
EN      38    50    POLY(1)   21    98    0.78925     1
M15     40    39    99   99   POX  L=1.5U     W=1500U
M16     40    38    50   50   NOX  L=1.5U     W=1500U
C15     40    39    50P
C16     40    38    50P
.MODEL DX D(RS=1 CJO=0.1P)
.MODEL NIX NMOS(VTO=0.75 KP=205.5U RD=1 RS=1 RG=1 RB=1
+CGSO=4E-9
+CGDO=4E-9 CGBO=16.667E-9 CBS=2.34E-13 CBD=2.34E-13)
.MODEL NOX NMOS(VTO=0.75 KP=195U RD=.5 RS=.5 RG=1 RB=1
+CGSO=66.667E-12
+CGDO=66.667E-12 CGBO=125E-9 CBS=2.34E-13 CBD=2.34E-13)
.MODEL PIX PMOS(VTO=-0.75 KP=205.5U RD=1 RS=1 RG=1 RB=1
+CGSO=4E-9
+CGDO=4E-9 CBDO=16.667E-9 CBS=2.34E-13 CBD=2.34E-13)
.MODEL POX PMOS(VTO=-0.75 KP=195U RD=.5 RS=.5 RG=1 RB=1
+CGSO=66.667E-12
+CGDO=66.667E-12 CGBO=125E-9 CBS=2.34E-13 CBD=2.34E-13)
.ENDS
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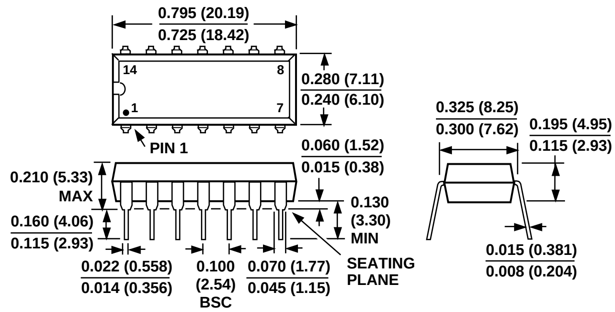
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

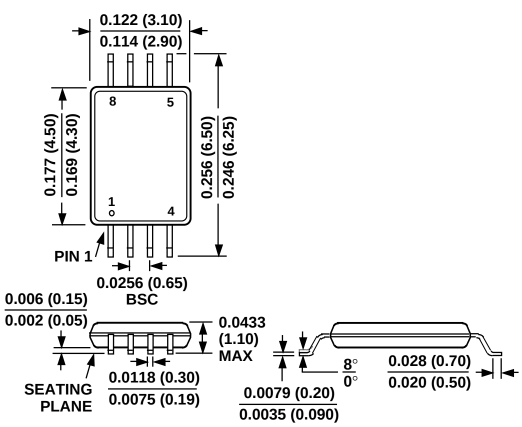
### 8-Pin Plastic DIP (N-8)



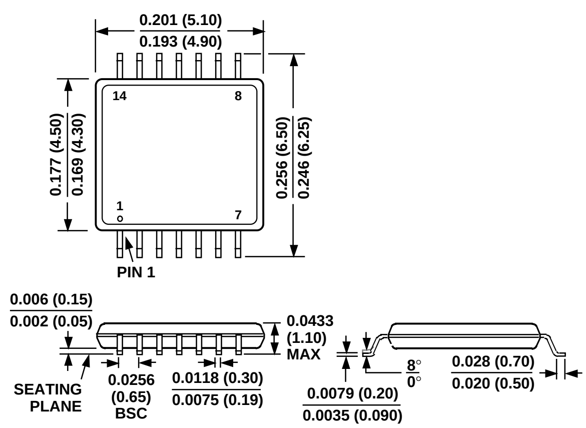

### 14-Pin Plastic DIP (N-14)




### 8-Pin TSSOP (RU-8)



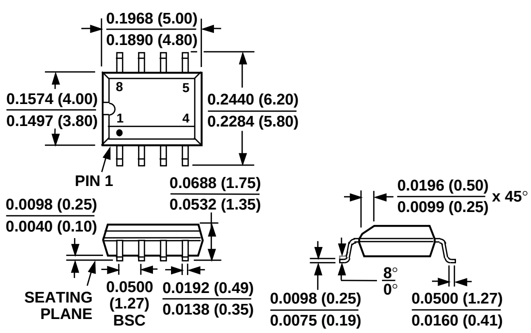

### 14-Pin TSSOP (RU-14)



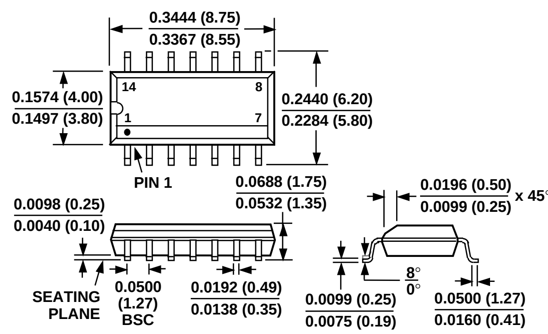
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

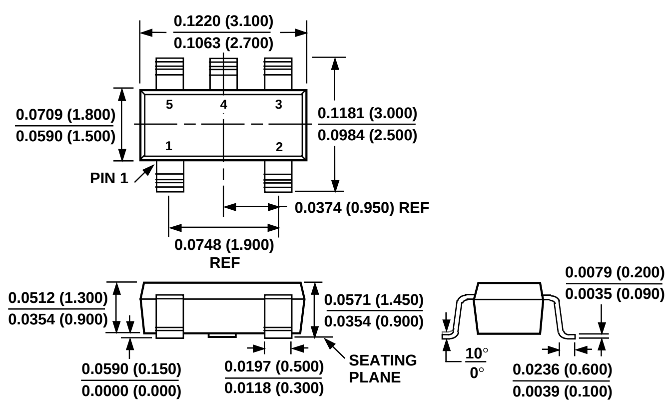
### 8-Pin SOIC (SO-8)




### 14-Pin SOIC (SO-14)




### 5-Lead SOT-23 (RT-5)




NOTE:
PACKAGE OUTLINE INCLUSIVE AS SOLDER PLATING.

C2149–18–7/96

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